

True rms Detector

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INTRODUCTION

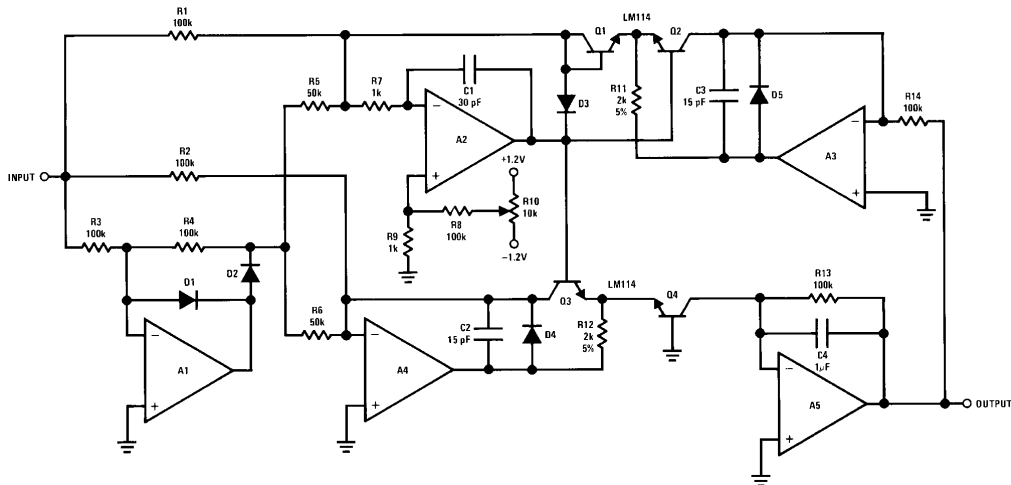
The op amp precision rectifier circuits have greatly eased the problems of AC to DC conversion. It is possible to measure millivolt AC signal with a DC meter with better than 1% accuracy. Inaccuracy due to diode turn-on and nonlinearity is eliminated, and precise rectification of low level signals is obtained.

Once the signal is rectified, it is normally filtered to obtain a smooth DC output. The output is proportional to the average value of the AC input signal, rather than the root mean square. With known input waveforms such as a sine, triangle, or square; this is adequate since there is a known proportionality between rms and average values. However, when the waveform is complex or unknown, a direct readout of the rms value is desirable.

The circuit shown will provide a DC output equal to the rms value of the input. Accuracy is typically 2% for a 20 V_{p-p}

input signal from 50 Hz to 100 kHz, although it's usable to about 500 kHz. The lower frequency is limited by the size of the filter capacitor. Further, since the input is DC coupled, it can provide the true rms equivalent of a DC and AC signal.

Basically, the circuit is a precision absolute value circuit connected to a one-quadrant multiplier/divider. Amplifier A1 is the absolute value amplifier and provides a positive input current to amplifiers A2 and A4 independent of signal polarity. If the input signal is positive, A1's output is clamped at -0.6V, D2 is reverse biased, and no signal flows through R5 and R6. Positive signal current flows through R1 and R2 into the summing junctions of A2 and A4. When the input is negative, an inverted signal appears at the output of A1 (output is taken from D2). This is summed through R5 and R6 with the input signal from R1 and R2. Twice the current flows through R5 and R6 and the net input to A2 and A4 is positive.



Note 1: All operational amplifiers are LM118.

Note 2: All resistors are 1% unless otherwise specified.

Note 3: All diodes are 1N914.

Note 4: Supply voltage $\pm 15V$.

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Amplifiers A2 through A5 with transistors Q1 through Q4 form a log multiplier/divider. Since the currents into the op amps are negligible, all the input currents flow through the logging transistors. Assuming the transistors to be matched, the V_{be} of Q4 is:

$$V_{be}(Q4) = V_{be}(Q1) + V_{be}(Q3) - V_{be}(Q2)$$

The V_{be} 's of these transistors are logarithmically proportional to their collector currents so

$$\log(I_{C4}) = \log(I_{C1}) + \log(I_{C3}) - \log(I_{C2})$$

$$\text{or } I_{C4} = \frac{I_{C1}I_{C3}}{I_{C2}}$$

where I_{C1} , I_{C2} , I_{C3} , and I_{C4} are the collector currents of transistors Q1–Q4.

Since I_{C1} equal I_{C3} and is proportional to the input, the square of the input signal is generated. The square of the input appears as the collector current of Q4. Averaging is done by C4, giving a mean square output. The filtered

output of Q4 is fed back to Q2 to perform continuous division where the divisor is proportional to the output signal for a true root mean square output.

Due to mismatches in transistors, it is necessary to calibrate the circuit. This is accomplished by feeding a small offset into amplifier A2. A 10V DC input signal is applied, and R10 is adjusted for a 10V DC output. The adjustment of R10 changes the gain of the multiplier by adding or subtracting voltage from the log voltages generated by the transistors. Therefore, both the resistor inaccuracies and V_{be} mismatches are corrected.

For best results, transistors Q1 through Q4 should be matched, have high beta, and be at the same temperature. Since dual transistors are common, good results can be obtained if Q1, Q2 and Q3, Q4 are paired. They should be mounted in close proximity or on a common heat sink, if possible. As a final note, it is necessary to bypass all op amps with 0.1 μ F disc capacitors.

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